Crestron **CGDMX-512BI / D**

Bi-directional DMX512 Interface
Operations Guide

Crestron Media Processor and DMX512 In
HTP / LTP or exclusive processed
to DMX512 Output
[single channel configurable]

DMX In or merge result to Crestron Media Processor
Inclusive RETIMER DMX512

CRESTRON

www.crestron-int.be

Index

Description

The CGDMX-512BI is a serial to DMX512 interface which makes easy interfacing possible between a CRESTRON control system and lighting products using the DMX512 protocol.

Only one serial RS-232/422 port on the Crestron control system is required to communicate with the DMX512 interface.

The DMX Interface has two separate DMX Ports, one **DMX Out** to send data to the DMX lighting products and one **DMX In** to receive data from e.g. DMX512 lighting consoles or other DMX512 control units.

The CGDMX-512BI can operate in different modes, to process the incoming DMX512 data with the Crestron data like HTP[1], LTP[2] and exclusive[3] handling. The Crestron media processor is able to change these modes, too. Furthermore the Crestron media processor can set the HTP, LTP and exclusive handling for each channel separately. See “Interface Modes”.

The CGDMX-512BI interface processes the incoming DMX512 data byte by byte, as fast as possible. This method features delay times between an incoming DMX512 channel and its leaving of only 44µs up to 20ms at a RETIMER setting 0.

In the following “Crestron Media Processor” is abbreviated with **CMP.**

[1] HTP= highest takes precedence
[2] LTP= last takes precedence
[3] excl. = DMX value or Crestron value takes precedence

Plug Connectors and Status-LED's

1) DMX512 Output [+Data (3), GND_2 (1), -Data (2)]

2) DMX512 Input [+Data (3), GND_1 (1), -Data (2)]

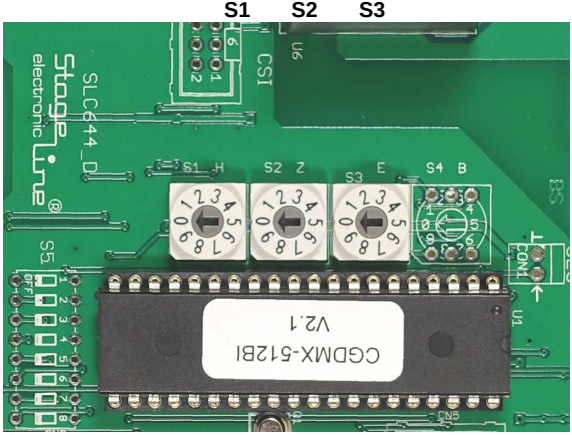
3) Status LED's
"CN COM" shows traffic between CMP and CGDMX-512BI
"DMX512" = ON - shows valid DMX512 input signal
blink - no DMX512 Input

4) RS232/422 Interface-connector to CMP
Asymmetrical or symmetrical wiring is available by Jumper J5.

TX	(RS232)	= pin 2	RTS (RS232)	= pin 7
RX	(RS232)	= pin 3	CTS (RS232)	= pin 8
GND_3	(RS232/422)	= pin 5		
TX-	(RS422)	= pin 1	RX- (RS422)	= pin 9
TX+	(RS422)	= pin 6	RX+ (RS422)	= pin 4

Rotary Code Switches [inside CGDMX-512BI]

S1: Baud rate (1200 to 115200 bit/s, this page) */factory 7*
S2: DMX512 Speed (44 to 20 frames/s, page 14) */factory 1*
S3: Interface Modes (page 6) */factory 1*



Baud rate COM interface [set by S1]

0	1	2	3	4	5
1200	2400	4800	9600	14400	19200

6	***7***	8	9
28800	***38400***	76800	115200

The interface type - symmetrical RS422 or asymmetrical RS232 is selectable by Jumper J5 as printed on pcb. (here RS422 = RS485) (Factory setting RS232)

MODE select [by rotary code switch S3]

MODE	SHORTFORM / DESCRIPTION
0	**TX DMX512 only** XSIG values received from CMP - transmitted as DMX512 values. No DMX512 Input.
1	***RX/TX DMX512 + message on change*** XSIG values received from CMP - transmitted as DMX512 values. **!** every Data change on a single DMX512 channel will be transmitted to CMP as an 4 byte XSIG value.
2	**RX/TX DMX512, HTP Merge** HTP merge between DMX512-IN and CMP-values to DMX Output. **!** HTP configuration is changeable by CMP (HTP, LTP, Excl., each channel separately). **!** after Power-On or xFC (Interface-Reset) the CGDMX-Interface returns to HTP all channels.
3	**RX/TX DMX512, HTP Merge + message on change** HTP merge between DMX512-IN and CMP-values to DMX Output. **!** every data change on a single DMX512 channel will be transmitted to CMP as an 4 byte XSIG value. **!** HTP configuration is changeable by CMP (HTP, LTP, Excl. , each channel separately). **!** after Power-On or xFC (Interface Reset) the CGDMX-Interface returns to HTP on all channels.

MODE select [by rotary code switch S3]

MODE	SHORTFORM / DESCRIPTION
4	**RX/TX DMX512, LTP Merge** LTP merge between DMX512-IN and CMP-values to DMX Output. **!** LTP configuration is changeable by CMP (HTP, LTP, Excl. , each channel separately). **!** after Power-On and xFC (Interface Reset) the CGDMX-Interface returns to LTP all channels.
5	**RX/TX DMX512, LTP Merge + message on change** LTP merge between DMX512-IN and CMP-values to DMX Output. **!** every data change on a single DMX512 channel will be transmitted to CMP as an 4 byte XSIG value. **!** LTP configuration is changeable by CMP (HTP, LTP, Excl. , each channel separately). **!** after Power-On and xFC (Interface Reset) the CGDMX-Interface returns to LTP all channels.
6	**processing with configuration 0, Merge** reads complete 512 byte configuration from non volatile memory how to process values from DMX IN with CMP values to DMX Output. (MERGE -HTP, -LTP, -Excl., may set for each channel, see channel processing flags). **!** after Power-On and xFC (Interface Reset) the CGDMX-Interface returns to process config stored in “config0”.
7	**processing with configuration 1, Merge** reads complete 512 byte configuration from non volatile memory how to process values from DMX IN with CMP values to DMX Output. (MERGE -HTP, -LTP, -Excl., may set for each channel, see channel processing flags). **!** after Power-On and xFC (Interface Reset) the CGDMX-Interface returns to process config stored in “config1”.

MODE select [by rotary code switch S3]

MODE	SHORTFORM / DESCRIPTION
8	**Auto fade all channel** Test - all DMX channels are fade between 0-100%. **!** the values are also send to CMP as 4 Byte XSIG analog values.
9	**all channel 75%** Test - all DMX channels will set to 75%. **!** the values are also send to CMP as 4 Byte XSIG analog values.

MODE change - volatile [by CMP XSIG digital command]

- active in all Modes (selected by codeswitch)
- active process-bit mask “send selected DMX IN value on change”.
- mutual triggering 4086 - 4089

ADR	VALUE	DESCRIPTION
4086	~	DMX Out by CMP - complete universe controlled by CMP exclusive.
4087	~	DMX OUT by DMX IN - complete universe controlled by DMX IN exclusive [CMP special function]
4088	~	DMX-OUT = DMX-IN <HTP> CMP-OUT Complete Universe HTP merge between DMX-IN and CMP-OUT values.
4089	~	DMX-OUT = DMX-IN <LTP> CMP-OUT Complete Universe LTP merge between DMX-IN and CMP-OUT.
4090	0/1	OFF/ON complete process bit-mask in upper modes [auto send XSIG analog Value to CMP on value change]

Channel processing flags [by XSIG digital command]

(XSIG digital OUT)

ADR	VALUE	DESCRIPTION
1024 - 1535	~	DMX Out channel 1-512 processed by CMP exclusive
1536 - 2047	~	DMX Out channel 1-512 processed by DMX In only
2048 - 2559	~	DMX Out channel 1-512 as a result of HTP merge of CMP and DMX In channel
2560 - 3071	~	DMX Out channel 1-512 as a result of LTP merge of CMP and DMX In channel

! These bits has a mutual triggering.

(XSIG digital IN)

ADR	VALUE	DESCRIPTION
3072 - 3583	1/0	On a value change of the selected DMX IN channel, a 4 byte XSIG analog value is send to CMP.

ADR	VALUE	DESCRIPTION
4091	~	request all process flags 1024-3683 as an XSIG digital value.

Channel processing flag registers [by XSIG digital command]

Additional process configuration register [config0] and [config1] These non volatile registers contains an individual processing configuration for each of the 512 channels between CMP and DMX In. (see “single channel processing options”)

! On Power On and interface reset the CGDMX-512BI starts with the configuration as given in the selected Mode.
[Mode 6 uses config0, Mode 7 uses config1]

ADR	VALUE	DESCRIPTION
4082	~	copy the configuration bits from **config0** to “process config” work register. (sets the bits from Address 1024-3683)
4083	~	Write current “process config flags” to the **config0** register in non volatile Memory.
4084	~	Copy the configuration bits from **config1** to “process config” work register. (sets the bits from Address 1024-3683)
4085	~	Write current “process config flags” to the **config1** register in non volatile Memory.

Basic commands

xFC Interface Reset by CMP
! reset volatile changes to selected Mode (switch S3)

xFD send all DMX512 IN data, channel by channel, as 4 byte XSIG analog values to CMP.
Transmission time depends from CMP interface speed.

ADR	VALUE	DESCRIPTION
0 - 511	1/0	switches DMX out channel 1 - 512 to 100% / 0%
512 - 1023	1/0	switches DMX channel 1 - 512 in AUX buffer to 100% / 0%
4095	~	request valid DMX512 Input Signal and respond as XSIG digital value on Address 4095 [0 = no DMX512, 1 = valid DMX512]

(see flow chart on page 13)

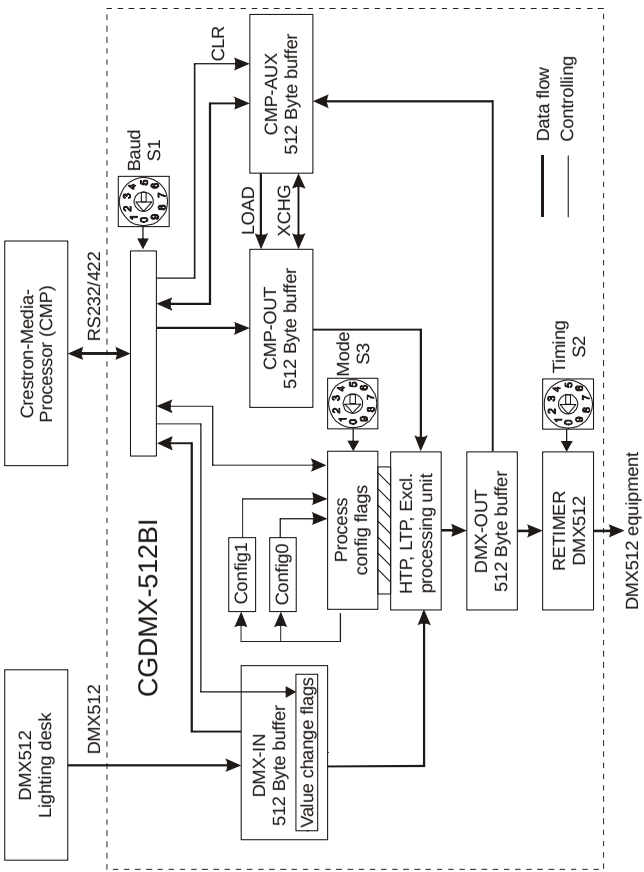
DMX-OUT buffer:
It contains the 512 bytes of the result of the processed CMP-OUT and DMX IN values.

CMP-OUT buffer:
It contains 512 bytes set by CMP to be processed with the DMX In data.

CMP-AUX buffer:
It contains 512 bytes for an individual use by CMP. Fast exchange with CMP-OUT buffer, fast load to CMP-Out buffer and as transfer buffer from fast DMX to slower COM interface.
["Snapshot" of DMX Out to CMP means copy of 512 bytes while incoming data from DMX In, CMP-AUX may have data of more than 1 frame.] (see section 5 on page 3)

ADR	VALUE	DESCRIPTION
4080		copies the DMX512-OUT buffer to the CMP-AUX buffer (512 bytes).
4081		copies the CMP-AUX buffer to the CMP buffer (512 bytes).
4079		Exchange the two buffers CMP-AUX and CMP-Out.
4077		Clear CMP-OUT buffer.
4078		Clear CMP-AUX buffer.
4092	~	send DMX-IN buffer to CMP as XSIG analog values (512 x 4 bytes)
4093	~	send CMP-AUX buffer to CMP as XSIG analog values (512 x 4 bytes)
4094	~	clear all DMX buffers

Data & Control flow chart

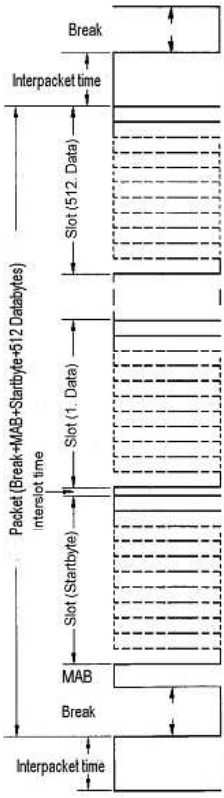


RETIMER DMX512 [adjustable DMX512 output timing, set by S2]

The DMX512 data are processed by the CGDMX-512BI interface with an optimal and standard-compliant DMX512 timing (as recommended in USITT DMX512A, American National Standard E1.11–2004 / 8.11 table 6 & 7 and DIN 56930-2 / 4.4.1.).
If problems should appear like flickering or short black outs, the connected lighting devices may be not able to receive DMX512 data with optimum timing..
In this case the CGDMX-512BI includes a RETIMER section to adjust the DMX512 timing to slower DMX devices.
You will find a DMX512 timing diagram on next site.

S2	BREAK (µs)	MAB (µs)	DATA (µs)	MBB (µs)	description
0	176	12	44	0	B2B 22,8ms !
1	***176***	***12***	***48***	***0***	***48 µs per byte***
2	176	12	48	176	48 µs & MBB 176 µs
3	176	12	52	0	52 µs
4	176	18	52	176	52 µs & MBB 176 µs
5	176	18	56	0	56 µs
6	176	18	56	352	56 µs & MBB 352 µs
7	176	18	64	352	64 µs & MBB 352 µs (30 frames / second)
8	176	18	77	528	77 µs & MBB 528 µs (25 frames / second)
9	176	18	96	528	96 µs & MBB 528 µs (20 frames / second)

MAB = Mark after Break
MBB = Mark before Break
B2B = Break to Break



DMX512 timing

Packet (22,7ms):
includes Break, MAB, startbyte and up to 512 data bytes.

Interpacket time:
time between two frames

Slot (44µs):
1 start-bit, data-byte (8Bit), 2 stop-bits

Interslot time:
time between two data bytes

Technical data

Supply voltage range:	85 - 305V~, 47- 440Hz
Power consumption:	approx. 5W
Fuse:	slow 0,63A -Type TR5
I/O 1:	RS232/422 (selectable)
I/O 2:	DMX512-A, terminated, 120ohm automatic switch after power on
Timing: (adjustable)	Break: 179µs Mark: 14µs B2B: 22,8ms (S2=0)
Isolation:	all I/O (DIN56930-2/4.2.3)
Weight:	approx. 480g
Dimensions:	200 x 110 x 57 mm (without plug connectors)
Case material:	UL-94-V-0, heavily inflammable
Revision:	D, V2.1 - starts with S/N:19.5686

Before opening, disconnect mains !

How to open CGDMX-512BI cover